HALF DENSITY ROM EMBEDDED DRAM

Technical Field of the Invention

[0001]   The present invention relates generally to memory devices and in particular the present invention relates to read only memory (ROM) embedded in a dynamic random access memory (DRAM).

Background of the Invention

[0002]   Semiconductor memory systems are comprised of two basic elements: memory storage areas and memory control areas. DRAM, for example, includes a memory cell array, which stores information, and peripheral circuitry, which controls the operation of the memory cell array.

[0003]   DRAM arrays are manufactured by replicating millions of identical circuit elements, known as DRAM cells, on a single semiconductor wafer. A DRAM cell is an addressable location that can store one bit (binary digit) of data. In its most common form, a DRAM cell consists of two circuit components: a storage capacitor and an access field effect transistor. The capacitor holds the value of each cell, namely a "1" or a "0," as a charge on the capacitor. Because the charge on a capacitor gradually leaks away, DRAM capacitors must be refreshed on a regular basis. A memory device incorporating a DRAM memory includes logic to refresh (recharge) the capacitors of the cells periodically or the information will be lost. Reading the stored data in a cell and then writing the data back into the cell at a predefined voltage level refreshes a cell. The required refreshing operation is what makes DRAM memory dynamic rather than static.

[0004]   The transistor of a DRAM cell is a switch to let control circuitry for the RAM either read the capacitor value or to change its state. The transistor is controlled by a row line coupled to its gate connection. In a read operation, the transistor is activated and sense amplifiers coupled to bit lines (column) determine the level of

charge stored in the memory cell capacitor, and reads the charge out as either a "1" or a "0" depending upon the level of charge in the capacitor. In a write operation, the sense amplifier is over-powered and the memory cell capacitor is charged to an appropriate level.

[0005]   Frequently, as in the case of microprocessors, microcontrollers, and other application specific integrated circuitry (ASICs), it is desired to incorporate read only memory (ROM) together with or in addition to RAM on a single semiconductor wafer. This typically requires the formation of separate additional peripheral circuitry and interconnects for the ROM. The ROM cells and additional circuitry require additional semiconductor wafer space and fabrication process steps that increase the overall costs of device fabrication.

[0006]   A read only memory (ROM) consists of an array of semiconductor devices (diodes, bipolar or field-effect transistors), which interconnect to store an array of binary data (ones or zeros). A ROM basically consists of a memory array of programmed data and a decoder to select the data located at a desired address in the memory array.

[0007]   Three basic types of ROMs are mask-programmable ROMs, erasable programmable ROMs (EPROMs) and field-programmable ROMs (PROMs). The data array is permanently stored in a mask-programmable ROM, at the time of manufacture, by selectively including or omitting the switching elements at the row-column intersections in the memory array. This requires a special mask used during fabrication of the integrated circuit, which is expensive and feasible only when a large quantity of the same data array is required. EPROMs use a special charge-storage mechanism to enable or disable the switching elements in the memory array. In this case, appropriate voltage pulses to store electrical charges at the memory array locations are provided. The data stored in this manner is generally permanent until it is erased using ultraviolet light allowing it to once again be programmed. PROMs are typically manufactured with all switching elements present in the array, with the connection at each row-column intersection being made by means of either a fuse element or an anti-fuse element. In

order to store data in the PROM, these elements (either the fuse or the anti-fuse, whichever are used in the design) are selectively programmed using appropriate voltage pulses supplied by a PROM programmer. Once the elements are programmed, the data is permanently stored in the memory array.

[0008] Programmable links have been used extensively in programmable read only memory (PROM) devices. Probably the most common form of programmable link is a fusible link. When a user receives a PROM device from a manufacturer, it usually consists of an X-Y matrix or lattice of conductors or semiconductors. At each cross-over point of the lattice a conducting link, call a fusible link, connects a transistor or other electronic node to this lattice network. The PROM is programmed by blowing the fusible links to selected nodes and creating an open circuit. The combination of blown and unblown links represents a digital bit pattern of ones and zeros signifying data that the user wishes to store in the PROM. By providing an address the data stored on a node may be retrieved during a read operation.

[0009] In recent years, a second type of programmable link, call an anti-fuse link, has been developed for use in integrated circuit applications. Instead of the programming mechanism causing an open circuit as in the case with fusible links, the programming mechanism in an anti-fuse circuit creates a short circuit or relatively low resistance link. Thus the anti-fuse link presents an open circuit prior to programming and a low resistance connection after programming. Anti-fuse links consist of two electrodes comprised of conductive and/or semiconductive materials and having some kind of a dielectric or insulating material between them. During programming, the dielectric in between the conductive materials is broken down by predetermined applied voltages, thereby electrically connecting the conducting and/or semiconducting materials together.

[0010] Like RAM cells, ROM cells need to store either a data 1 or a data 0. Processing factors, however, may limit the ROM cell to only one program state. For the reasons stated above, and for other reasons stated below which will become apparent to

those skilled in the art upon reading and understanding the present specification, there is a need in the art for a ROM-embedded-DRAM which can be fabricated with single state ROM cells.

Summary of the Invention

[0011] The above-mentioned problems with ROM-embedded-DRAM and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0012] In one embodiment, a memory device comprises a read only memory (ROM) cell hard programmed to a first data state, a dynamic memory cell, and access circuitry to couple the ROM cell and the dynamic memory cell to differential digit lines.

[0013] In another embodiment, a half-density read only memory (ROM) embedded dynamic random access memory (DRAM) device comprises a DRAM array comprising first dynamic memory cells, a ROM array comprising hard programmed non-volatile memory cells and second dynamic memory cells. Sense amplifier circuitry is coupled to differential digit lines of the ROM array and word lines to access rows of the memory ROM array. Access circuitry couples one of the non-volatile memory cells and one of the second dynamic memory cells to the differential digit lines in response to a pair of word line signals.

[0014] A method of operating a read-only memory comprises programming a first memory cell in a non-volatile manner to a first data state, providing an un-programmed volatile memory cell, and accessing both the first and second memory cell capacitors in response to word line signals.

Brief Description of the Drawings

[0015] Figure 1 is a simplified block diagram of a ROM embedded DRAM of an embodiment of the present invention; and

[0016] Figure 2A illustrates a pair of complementary digit lines of an embodiment of the memory of Figure 1; and

[0017] Figure 2B illustrates a pair of complementary digit lines of another embodiment of the memory of Figure 1.

Detailed Description of the Invention

[0018] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0019] Referring to Figure 1, a simplified block diagram of a ROM embedded DRAM 100 of the present invention is described. The memory device can be coupled

to a processor 110 for bi-directional data communication. The memory includes an array of memory cells 112. The array includes a dynamic (DRAM) portion 120 and a read only (ROM) portion 122. The ROM array is "embedded" in the dynamic memory and may include some dynamic cells. Control circuitry 124 is provided to manage data storage and retrieval from the array in response to control signals 140 from the processor. Address circuitry 126, X-decoder 128 and Y-decoder 130 analyze address signals 142 and storage access locations of the array. Sense circuitry 132 is used to read data from the array and couple output data to I/O circuitry 134. The I/O circuitry operates in a bi-directional manner to receive data from processor 110 and pass this data to array 112. It is noted that the sense circuitry may not be used in some embodiments to store the input data.

[0020]   Dynamic memories are well known, and those skilled in the art will appreciate that the above-described ROM embedded DRAM has been simplified to provide a basic understanding of DRAM technology and is not intended to describe all of the features of a DRAM. The present invention uses the basic architecture and fabrication techniques of a DRAM and provides an embedded ROM array for non-volatile storage of data. This data can be used to store boot-type data for a system, a non-volatile look-up table, or other data that does not require a dedicated ROM memory device. Embedding ROM storage in a DRAM is most economically beneficial if the DRAM is not substantially altered during fabrication or operation. That is, small fabrication changes allow the embedded memory to be fabricated using known techniques. Further, it is desired to maintain operation of the memory in a manner that is externally transparent. As such, an external processor, or system, does not need special protocol to interface with the embedded memory.

[0021]   One technique for physically programming ROM embedded cells is described in U.S. Patent No. 6,134,137 issued October 17, 2000 entitled "ROM-Embedded-DRAM", incorporated herein by reference. U.S. Patent No. 6,134,137 teaches that slight modifications in fabrication masks allow DRAM cells to be hard

programmed to Vcc or Vss by shorting the cell to wordlines. The memory reads the ROM cells in a manner that is identical to reading the DRAM cells. As described below, the present invention provides an improved ROM embedded DRAM.

[0022]   As explained above, conventional ROM devices program two data states, logic 1 and 0. When the memory cells are read, therefore, both data states are readily available. In contrast, the present invention provides a combination ROM and DRAM memory device. The ROM memory cells can be programmed to only one data state. This is accomplished by shorting selected ROM cells to one voltage to remain programmed in a non-volatile manner.

[0023]   Referring to Figure 2A, a simplified schematic diagram of an embodiment of the present invention is described. The memory includes dynamic memory cells 151 and 152 that can be selectively coupled to complimentary digit lines 160 and 162. The digit lines can be electrically coupled to sense amplifier circuitry 170 to detect a voltage differential between the digit lines. Additionally, a pre-charge/equilibrate circuit 172 can be provided to balance the digit lines to a predetermined voltage, such as Vcc/2. Memory cells are hard programmed, as explained below, to operate as a non-volatile ROM cells.

[0024]   Numerous methods are available to program the ROM cells. For example, U.S. Patent No. 6,134,137 issued October 17, 2000 entitled "ROM-EMBEDDED-DRAM" describes ROM cells that are fabricated to short the memory cell to either its wordline of an adjacent wordline. Shorting the memory cell to its wordline results in reading a logic one (Vcc). Shorting the memory cell to an adjacent wordline results in reading a logic zero (Vss). Shorting a cell to its own wordline, however, may result in a digit line to wordline short during fabrication. As such, hard programming logic zeros may only be possible for some fabrication layouts. The hard programming technique of U.S. Patent No. 6,134,137 is an example of a technique for programming ROM cells using a DRAM fabrication. Other techniques for programming a ROM cell using a DRAM fabrication can be used without departing from the present invention. For

example, ROM cells can be hard programmed by eliminating cell dielectric so that the cell plates are shorted to a program voltage, an electrical plug can be fabricated between the cell plates and shorted to a program voltage, the ROM cell can be programmed using an anti-fuse programming technique, the ROM cells can also be programmed by providing a high leakage path (not full short) such as through an active area to the substrate.

[0025]   The embodiment of Figure 2A uses two memory cells 151 and 152 to store a bit of data. One of the memory cells is a hard programmed ROM cell and the second cell is a dynamic cell, such as a non-programmed ROM bit that had to be skipped because the ROM cells are only programmed to one polarity. As a result, half of the cells in the ROM portion of the array are skipped in order to use the Half Density option to store ROM bits that represent both "1" and "0" data states. Thus, the ROM cell can be programmed to provide either a logic one or a logic zero. For example, memory cell 151_1 and memory cell 152_n are hard programmed to ground (Vss). In operation, word lines WL1 and WL2 are activated together to access both memory cell 151_1 and 152_1. In response, digit line 160 is pulled to ground and digit line 162 remains at the precharge level, Vcc/2. The sense amplifier detects this differential between the digit lines and provides a logic one output. In contrast, when word lines WL3 and WL4 are activated, digit line 162 is pulled to ground and digit line 160 remains at the precharge level, Vcc/2. The sense amplifier detects this differential between the digit lines and provides a logic zero output.

[0026]   The embodiment of Figure 2B uses two memory cells 151 and 152 to store a bit of data. One of the memory cells is a hard programmed ROM cell and the second cell is a dynamic cell, such as DRAM capacitor cell. The ROM cell can be programmed to provide either a logic one or a logic zero. For example, memory cell 151_1 and memory cell 152_n are hard programmed to Vcc. In operation, word lines WL1 and WL2 are activated together to access both memory cell 151_1 and 152_1. In response, digit line 160 is pulled to Vcc and digit line 162 remains at the precharge level, Vcc/2. The sense

amplifier detects this differential between the digit lines and provides a logic one output. In contrast, when word lines WL3 and WL4 are activated, digit line 162 is pulled to Vcc and digit line 160 remains at the precharge level, Vcc/2. The sense amplifier detects this differential between the digit lines and provides a logic zero output.

Conclusion

[0027] A half-density ROM embedded DRAM has been described. The memory provides ROM cells that can be programmed to a single state. By hard programming either a first or second memory cell in a pair of cell, different data states are stored. Two word lines are used to access the memory cell pair. Because one of the cells is hard programmed, sense amplifier circuitry identifies the appropriate data state. The ROM cell can be programmed in numerous different manners. For example, ROM cells can be hard programmed by eliminating cell dielectric to short cell plates to a program voltage, or an electrical plug can be fabricated between the cell plates and shorted to a program voltage. In other embodiments, the ROM cell can be programmed using an anti-fuse programming technique, or by providing a high leakage path (not full short) such as through an active area to the substrate.

[0028] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.